a plurality of gates of the unit cells, the plurality of gates being electrically connected in parallel and having a non-uniform spacing between the gates, wherein the non-uniform spacing between the gates is provided in a pattern that provides a lower peak junction temperature during RF operation than a corresponding uniform gate pitch device for a particular set of operating conditions.

16. (Original) The field effect transistor of Claim 15, wherein the plurality of unit cells comprise a linear array of unit cells.

17. (Original) The field effect transistor of Claim 15, wherein the plurality of unit cells comprise a two dimensional array of unit cells.

18. (Original) The field effect transistor of Claim 17, wherein the non-uniform spacing of the gates is in a single dimension of the two dimensional array.

19. (Original) The field effect transistor of Claim 17, wherein the non-uniform spacing of the gates is in both dimensions of the two dimensional array.

20. (Original) The field effect transistor of Claim 15, wherein the plurality of unit cells comprise a plurality of silicon carbide unit cells.

21-27. Canceled.

28. (Previously presented) The field effect transistor of Claim 15, wherein the spacing between the gates is at least 60 μm, and wherein the field effect transistor is capable of producing at least 30 W of RF output power.

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29 ~~28~~. (Previously presented) The field effect transistor of Claim 15, wherein the spacing between the gates is at least 40 μm, and wherein the field effect transistor is capable of producing at least 60 W of RF output power.

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~~29~~. (Previously presented) The field effect transistor of Claim 15, wherein the spacing between the gates varies in a substantially linear pattern from a small pitch to a larger pitch toward the center of the device.